Claims

[c1] 9. A fabrication method for a read only memory device, comprising:

providing a substrate, the substrate comprises a memory cell region and a periphery circuit region, wherein a memory cell array is formed in the memory cell region and a plurality of transistors is formed in the periphery circuit region;

forming a negative photoresist layer on the memory cell region;

performing a first exposure process to transfer a pattern in a first photomask to the negative photoresist layer, wherein the pattern in the first photomask corresponds to each memory cell in the memory cell region, and a non-crosslinked portion of the negative photoresist layer is positioned above the channel region of each memory cell in the memory cell region;

performing a second exposure process to transfer a pattern in a second photomask to the negative photoresist layer, wherein the pattern of the second photomask precisely corresponds to at least one pre-coding memory cell region in the memory cell region and the gates of the transistors in the periphery circuit region, and non-

crosslinked portions of the photoresist layer are positioned above the pre-coding memory cell region in the memory cell region and above the gates of the transistors in the periphery circuit region;
performing a development process to pattern the negative photoresist layer; and
performing an ion implantation process to the pre-coding memory cell region and to adjust a threshold voltage of the transistors using the patterned negative photoresist layer as a mask.

[c2] 10. The method of claim 9, wherein the first photomask includes a precise photomask.

[c3] 11. A method for coding a semiconductor device, the method comprising:
providing a substrate, the substrate comprises a coding region and a periphery circuit region, wherein a plurality of coding units are formed in the memory cell region and a plurality of transistors is formed in the periphery circuit region;
forming a negative photoresist layer on the substrate;
performing a first exposure process to transfer a pattern of a first photomask to the negative photoresist layer, wherein the pattern of the first photomask corresponds to at least one pre-coding regions in the coding region and the gates of the transistors in the periphery circuit

region, wherein a non-crosslinked portion of the negative photoresist layer is positioned above the the pre-coding region in the memory cell region and the gates of the transistors in the periphery circuit region, and the pre-coding region comprises at least one coding unit;
performing a second exposure process to transfer a pattern of a second photomask to the negative photoresist layer, wherein a pattern of the second photomask precisely corresponds to the coding units in the coding region, and non-crosslinked portions of the first negative photoresist layer are positioned above the coding unit within the pre-coding region;
performing a development process to pattern the negative photoresist layer; and
performing an ion implantation process to code the pre-coding unit in the pre-coding region and to adjust a threshold voltage of the transistors using the patterned negative photoresist layer as a mask.

[c4] 12. The method of claim 11, wherein the second photomask includes a precise mask.